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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,292	02/15/2002	Ludger Mimberg	NVID-P000406	3407

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EXAMINER	
SUN, XIUQIN	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,292	MIMBERG ET AL.	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- *The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/18/2004 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 9-10, 14, 17-18, 22, 25, 26, 30, 33, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch et al. (U.S. Pat. No. 6304824) in view of Talbot et al. (U.S. Pat. No. 6448815).

Bausch et al. teach a processor power supply voltage controller (see Abstract) comprising: an on-chip temperature sensor configured to sense a temperature of a processor and generate a temperature signal in accordance therewith (col. 5, lines 58-67; col. 6, lines 53-62 and col. 7, lines 14-40); and a regulator coupled to provide a

power supply voltage to the processor, the regulator coupled to receive the temperature signal and control the power supply voltage (col. 3, lines 18-25, lines 47-55; col. 4, lines 43-67; col. 5, lines 58-67; col. 6, lines 1-4, and lines 53-62). Bausch et al. further teach that: said temperature sensor further comprises a thermal diode circuit (col. 7, lines 41-52).

Bausch et al. further teach a system for regulating power supply voltage within an electronic device over a variable temperature range (see Abstract), said system comprising: a voltage supply circuit for supplying an output voltage to said electronic device (col. 3, lines 64-66 and col. 4, lines 29-32); and a temperature sensitive element coupled to said voltage supply circuit (col. 5, lines 58-67; col. 6, lines 53-62 and col. 7, lines 14-40); regulating said output voltage of said voltage supply circuit, wherein said voltage supply circuit increases said output voltage in response to a temperature increase and wherein said voltage supply circuit decreases said output voltage in response to a temperature decrease (col. 3, lines 18-25, lines 47-55; col. 4, lines 43-67; col. 5, lines 58-67; col. 6, lines 1-4, and lines 53-62). Bausch et al. further teach that: said electronic device is a semiconductor device (col.3, lines 2-4 and col. 5, lines 44-50); said temperature sensitive element is a thermistor (col. 7, lines 14-40).

Bausch et al. further teach an electronic system comprising: a semiconductor device operated over a variable temperature range (col. 3, lines 1-5, lines 47-55 and col. 5, lines 44-50); a voltage supply circuit supplying an output voltage to said semiconductor device for supplying power thereto (col. 3, lines 64-66 and col. 4, lines 29-32); and a temperature sensitive element coupled to said voltage supply circuit (col.

5, lines 58-67; col. 6, lines 53-62 and col. 7, lines 14-40); regulating said output voltage of said voltage supply circuit, wherein said voltage supply circuit, in response to said temperature sensitive element, increases said output voltage when said temperature increases and wherein said voltage supply circuit, in response to said temperature sensitive element, decreases said output voltage when said temperature decreases (col. 3, lines 18-25, lines 47-55; col. 4, lines 43-67; col. 5, lines 58-67; col. 6, lines 1-4, and lines 53-62).

Bausch et al. further teach a method of regulating power supply voltage (see Abstract) comprising: operating said electronic device over a variable temperature range (col. 3, lines 1-5, lines 47-55); detecting an ambient temperature adjacent to said electronic device (col. 7, lines 14-40); in response to said detecting, increasing a voltage supplied to said electronic device if said ambient temperature increases; and in response to said detecting, decreasing said voltage supplied to said electronic device if said ambient temperature decreases (col. 3, lines 18-25, lines 47-55; col. 4, lines 43-67; col. 5, lines 58-67; col. 6, lines 1-4, and lines 53-62). Bausch et al. further teach that: said step of detecting an ambient temperature is performed by a temperature sensitive element disposed near said electronic device (col. 7, lines 14-40); and said electronic device is a semiconductor device (col. 3, lines 1-5 and col. 5, lines 44-50).

Bausch et al. further teach an electronic system comprising: a semiconductor device operated over a variable temperature range (col. 3, lines 1-5, lines 47-55 and col. 5, lines 44-50); a voltage supply circuit supplying an output voltage to said semiconductor device for supplying power thereto (col. 3, lines 64-66 and col. 4, lines

29-32); and a temperature sensitive element coupled to said voltage supply circuit (col. 7, lines 14-40) and for regulating said output voltage of said voltage supply circuit, said temperature sensitive element configured for detecting an ambient temperature adjacent to said semiconductor device and in response to said detecting, increase said output voltage if said ambient temperature increases and decrease said output voltage supplied to said semiconductor device if said ambient temperature decreases (col. 3, lines 18-25, lines 47-55; col. 4, lines 43-67; col. 5, lines 58-67; col. 6, lines 1-4, and lines 53-62).

Bausch et al. further teach a system for regulating power supply voltage within an electronic device over a variable temperature range (see Abstract), said system comprising: a voltage supply circuit for supplying an output voltage to said electronic device (col. 3, lines 64-66 and col. 4, lines 29-32); a feedback circuit coupled to said voltage supply circuit (col. 5, lines 58-67 and col. 7, lines 14-40); and a temperature sensitive element (col. 7, lines 14-40) coupled to said voltage supply circuit and said feedback circuit for detecting a temperature of said electronic device and for regulating said output voltage of said voltage supply circuit, said voltage supply circuit configured to increase said output voltage in response to said feedback circuit signaling a temperature increase and decrease said output voltage in response to said feedback circuit signaling a temperature decrease (col. 3, lines 18-25, lines 47-55; col. 4, lines 43-67; col. 5, lines 58-67; col. 6, lines 1-4, and lines 53-62).

Bausch et al. don not mention explicitly that: said voltage supply circuit controls the power supply voltage to maintain a substantially stable crosstalk level within the processor.

Talbot et al. teach a voltage supply circuit that is capable of controlling the power supply voltage of a processor to maintain a substantially stable crosstalk level within the processor (col. 1, lines 25-32, lines 53-67; col. 2, lines 1-3, lines 38-51; col. 4, lines 35-58; col. 5, lines 9-19; and cols. 6-7, lines 3-9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Talbot et al. in the Bausch system and method in order to reduce the crosstalk level within the processor caused by the fluctuation of the power supply voltage (col. 1, lines 25-32 and col. 2, lines 38-51).

4. Claims 2, 3, 13, 21, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch et al. in view of Talbot et al., as applied to claims 1, 9, 17 and 25 above, and further in view of Hunsdorf et al. (U.S. Pat. No. 5757172).

Bausch et al. and Talbot et al. teach a processor power supply voltage controller, a system and method for maintaining a crosstalk level within an electronic device that includes the subject matter discussed above. Bausch et al. and Talbot et al. do not mention: said temperature sensor further comprises a negative temperature coefficient (NTC) resistor; a feedback circuit coupled to the negative temperature coefficient resistor, said feedback circuit configured to generate the temperature signal for the regulator.

Hunsdorf et al. disclose a voltage regulator coupled to a temperature sensor (see Abstract), and teach: said temperature sensor comprises a negative temperature coefficient (NTC) resistor, and a feedback circuit coupled to the negative temperature coefficient resistor, said feedback circuit configured to generate the temperature signal for the regulator (col. 3, lines 27-50 and col. 4, lines 9-13).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Hunsdorf et al. in the combination of Bausch and Talbot et al. in order to automatically adjust the voltage linearly based on the output from the temperature sensor (Hunsdorf et al., col. 1, lines 54-67; col. 2, lines 1-5 and col. 3, lines 27-50).

5. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch et al. in view of Talbot et al., as applied to claim 1 above, and further in view of Lee et al. (U.S. Pub. No. 20010045779 A1).

Bausch et al. and Talbot et al. teach a processor power supply voltage controller and a system and method for maintaining a crosstalk level within an electronic device that includes the subject matter discussed above. Bausch et al. and Talbot et al. do not mention: said temperature sensor is configured to sense the temperature of the processor by sensing a temperature of a heat sink coupled to the processor; said temperature sensor is configured to sense the temperature of the processor by sensing a temperature of an enclosure including the processor.

Lee et al. disclose an intelligent power system, and suggest to monitor the temperature of the peripherals that utilize the power supply by sensing a temperature of

a heat sink coupled to the peripherals as well as a temperature of an enclosure including the device that utilizes the power supply (section 0013, and section 0020, lines 10-17).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Lee et al. in the combination of Bausch and Talbot et al. in order for the voltage controller to collect as much information as possible from the peripherals that utilize the power supply to regulate the voltage supply more intelligently (Lee et al., sections 0004 and 0013).

6. Claims 7, 11, 15, 19, 23, 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch et al. in view of Talbot et al., as applied to claims 1, 9, 17 and 25 above, and further in view of Reinhardt et al. (U.S. Pat. No. 5745375).

Bausch et al. and Talbot et al. teach a processor power supply voltage controller and a system and method for maintaining a crosstalk level within an electronic device that includes the subject matter discussed above. Bausch et al. and Talbot et al. do not mention: said temperature sensor is configured to sense the temperature of the processor by sensing a die temperature of the processor; said semiconductor device is a central processing unit (CPU); and said voltage supply circuit is a switch mode power supply circuit.

Reinhardt et al. teach a power control circuit, including: a temperature sensor configured to sense the temperature of a processor of a central processing unit (CPU) by sensing a die temperature of the processor (col. 4, lines 31-45); said voltage supply circuit is a switch mode power supply circuit (col. 4, lines 64-67 and col. 5, lines 1-14).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Reinhardt et al. in the combination of Bausch and Talbot et al. in order to provide a power control circuit that can be used by any type of electronic devices (Reinhardt et al., col. 2, lines 5-9).

7. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch et al. in view of Talbot et al., as applied claim 33 above, and further in view of Brown (U.S. Pat. No. 5568350).

Bausch et al. and Talbot et al. teach a processor power supply voltage controller and a system and method for maintaining a crosstalk level within an electronic device that includes the subject matter discussed above. Bausch et al. and Talbot et al. do not mention: said regulator is coupled to provide the power supply voltage to a plurality of power supply voltage inputs of the processor.

Brown discloses a power supply system including a regulator, and said regulator is coupled to the power supply voltage to provide a plurality of power supply voltage inputs of a processor (col. 2, lines 30-52).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Brown in the combination of Bausch and Talbot et al. in order to provide a plurality of voltage levels required by the processor (Brown, col. 2, lines 30-52).

8. Claims 12, 16, 20, 24 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch et al. in view of Talbot et al., as applied claims 9, 17 and 25 above, and further in view of Patel et al. (U.S. Pat. No. 6025737).

Bausch et al. and Talbot et al. teach a processor power supply voltage controller and a system and method for maintaining a crosstalk level within an electronic device that includes the subject matter discussed above. Bausch et al. and Talbot et al. do not mention: said semiconductor device is a graphics processing unit; and said temperature sensitive element, said voltage supply circuit and said electronic device are all mounted on a common electronic PC board.

Patel et al. disclose a circuit for low internal voltage integrated circuit, and teach that: said integrated circuit is a graphics processing unit (col. 4, lines 34-41); and a voltage supply circuit and said integrated circuit are all mounted on a common electronic PC board (col. 2, lines 3-26; col. 3, lines 66-67 and col. 4, lines 1-21).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Patel et al. in the combination of Bausch and Talbot et al. in order to provide an on-chip voltage supply circuit that can be utilized by any type of processing unit (Patel et al., col. 2, lines 3-50).

Response to Arguments

9. Applicant's arguments with respect to claims 1-7 and 9-36 dated February 18, 2004 have been considered but are moot in view of the new ground(s) of rejection.

Applicant(s) filed a declaration on 02/18/2004, in which applicants submitted evidence proving that the instant application has a filing date earlier than that of the U.S. Pub. No. 20020113622 used in office action dated 11/12/2003, therefore disqualifying this reference for any art rejection of the instant application. Examiner conducted an

updated search and found U.S. Pat. No. 6448815. This reference was used in this office action in lieu of the disqualified U.S. PUB. No. 20020113622. A detailed office action is set forth as discussed above.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Xiuqin Sun
Examiner
Art Unit 2863

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